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METHOD AND APPARATUS FOR SWITCHING DATA BETWEEN BITSTREAMS OF A CIRCUIT SWITCHED TIME DIVISION MULTIPLEXED NETWORK

Technical field of the invention

The present invention refers to a method and an apparatus for switching data between bitstreams of a circuit switched synchronous time division multiplexed network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots.

Technical Background and Prior Art

Today, new types of circuit-switched communication networks are being developed for the transfer of information using synchronous or isochronous, time division multiplexed bitstreams, wherein a bitstream is divided into cycles, each cycle in turn being divided into time slots.

An example of such a network is described in "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994, and in "Multi-gigabit networking based on DTM", Lars Gauffin, Lars Håkansson, and Björn Pehrson, Computer networks and ISDN Systems, 24(2):119-139, April 1992.

The basic topology of a network of this kind is preferably a bus with two unidirectional, multi-access optical fibers connecting a number of nodes, each node being arranged to serve one or more end users connected thereto. Note, however, that the topology may just as well be realized by any other kind of structure, e.g. a ring structure or a hub structure.

The bandwidth of each wavelength on the bus, i.e. each bitstream on each fiber, is divided into cycles with fixed cycle rate, which cycles in turn are divided into fixed size time slots. The number of slots in a cycle

thus depend on the network's bit-rate. The time slots are divided into two groups, control slots and data slots. Control slots are used for transferring of signaling messages between said nodes for the network's internal operation. The data slots are used for the transfer of data between said users connected to the different nodes.

Each node is arranged to dynamically allocate time slots for its respective end users to use when sending or receiving information to or from other users. As a result, different end users have write access to different data slots.

When, for example, a first user connected to a first node wants to transfer information to a second user connected to a second node, said first node will allocate a number of data slots within each cycle for the first user to write data into. The first node will also send a control message in a control slot to the second node, instructing said second node to read any data being provided in said allocated data slots within said cycle and to send such data to said second user. Said allocated data slots is referred to as a channel between the two users.

In such a network, so called switch nodes, each connected to two or more bitstreams, or fibers, are used to switch time slot data between different bitstreams. For example, a channel between a first and a second end users connected to a first and a second, respectively, node on a first and a second, respectively, fiber is defined by a first set of time slots on a bitstream propagating on the first fiber and a second set of slots on a bitstream propagating on the second fiber, and the switch node is then used to transfer or copy time slot data from time slots of the first set of slots to time slots of the second set of slots, or vice versa.

According to prior art, switch nodes in synchronous time division multiplexed networks use a control memory that maps each incoming slot number to the outgoing slot number. Such mapping may involve both a mapping in the

time domain, i.e. control of the order in which time slot data are written into each bitstream, and a mapping in the space domain, i.e. controlling which time slot data goes to which bitstream. For example, so called time-space-time (TST) switches are described in "Data and Computer Communications", 4th ed., by Williams Stallings, Macmillan Publishing Company. However, prior art switches all show limitation as to the possibilities of switching time slots in space and time. Also, prior art switches show limitations as to switching speed and capacity.

Objects of the invention

An object of the invention is therefore to provide a switch which provides greater freedom as to the possibilities of switching time slots in space and time.

Another object of the invention is to increase the switching speed and capacity.

Summary of the invention

The above mentioned and other objects are achieved by the invention as defined in the accompanying claims.

Hence, according to a first aspect of the invention, there is provided a method of the kind mentioned in the introduction, further comprising the steps of: tagging time slot data read from a time slot of a first bitstream of said bitstreams with an identifier; and selecting, for each one of at least a second and a third bitstream of said bitstreams, whether or not said time slot data is to be transmitted thereto and, if so, into which time slot thereof, based upon said identifier.

Correspondingly, according to a second aspect of the invention, there is provided an apparatus of the kind mentioned in the introduction, comprising: associating means for tagging time slot data read from a time slot of a first bitstream of said bitstreams with an identifier; and selecting means for selecting, for each one of at least a second and a third bitstream of said bitstreams,

whether or not said time slot data is to be transmitted thereto and, if so, into which time slot thereof, based upon said identifier.

The invention is thus based upon the idea of tagging incoming time slot data with a tag, forming said identifier, for example in the form of a virtual tag number, which is then used for each output port in the decision as to whether or not the respective time slot data is to be transmitted to the respective outgoing bitstream and, if so, as to which time slot position of the respective output bitstream that said time slot data shall be transmitted into. Incoming slots are thus sent to the outgoing ports without any direct specification of what slots to use on the outgoing link. Hence, the decision as to which slot to use on the outgoing link for the time slot data is thus made at the output port and not at the input port. As is understood, said identifier will generally not be the actual slot number to which the data slot is supposed to be written.

An advantage of the invention is that the input ports of a switch according to the invention does not have to perform the decision as to which slot goes where, i.e. does not have to tag said time slot data with different port and slot addresses for different ports and slots. This is a great advantage in a multicasting situation, since the input port does not have to specify which (one or more) output port that a specific time slot data shall be sent to. Instead, the input port merely provides the time slot data with a single identifier, e.g. said virtual tag number. The time slot data, along with said identifier, is then sent to the output ports, either using a shared resource or private links, where the actual decisions as to write the time slot data into an outgoing time slot are made. Thus, several output ports will make their decisions based upon the same identifier. This feature is very beneficial in space multicasting.

The information as to which identifiers that are to be used for which time slots and how the respective time slots are to be switched is provided by a node controller, which performs control signaling with the outside network and which will make the necessary allocations and provide the necessary instructions at channel set-up, modification and termination.

In one embodiment, incoming time slot data is provided to each output port, thus letting each output port make a decision for each received time slot data as to whether or not said time slot data is supposed to be transmitted to the respective bitstream. In this embodiment, the transfer of time slot data from input port to output port comprises no intermediate desicionmaking, however there is required a larger decisionmaking capacity at each output port.

In an alternative embodiment, the decisionmaking is divided into subselections, comprising first selecting which ones (one or more) of the output bitstreams that said time slot data is to be transferred to, based upon said an identifier, and then selecting, for each one of the first selected bitstreams, a respective time slot for said time slot data to be written into, based upon said identifier. Note that said identifier is used as a basis for both subselections. This embodiment requires that further decisionmaking schemes are provided, but also puts a lesser demand on the decisionmaking capacity at the respective output port.

It shall be understood that space multicasting according to the invention, i.e. the switching of time slot data from at least one input port to at least two output ports, may involve the selection of different single output ports for different input time slots, the selection of more than one output port for an input time slot as well as the selection of all output ports for said input time slot (broadcasting).

According to an embodiment of the invention, which is preferably used in the case when one or more copies of time slot data from a specific input time slot has to be provided within the node, all copies of the time slot data is tagged with the same tag number, forming said identifier. Hence, one single tag number will be used for an input time slot, independently of how many copies of the time slot data therefrom that are provided within the switch.

The time slot data, along with the identifier tagged thereto, may be transferred within the node using private links, shared multiplexed links, or the like. For example, said time slot data and said identifier may be transferred within said node using time slots of an internal bitstream.

According to a preferred embodiment of the invention, in a situation where an isochronous channel has been established on said bitstreams, said channel comprising a first set of time slots in the first bitstream and a second set of time slots in the second bitstream, time slot data from time slots of the input bitstream belonging to the same channel are tagged with the same identifier, e.g. the same virtual tag number. Said identifier is then used at the output port for mapping said time slot data to one of the time slots allocated to the channel on the outgoing link. Which time slot that the data is mapped to depends on which time slot passing the node next that has not yet been filled with switched data. In this embodiment one advantage is that the timing requirements between the incoming and the outgoing channels are relaxed, since it needs not be determined which specific incoming slot number that is mapped to which specific outgoing slot number at channel set-up. Instead, this is handled dynamically. In many applications, it is important, though, to make sure that the time slot data from time slots of said first set of time slots are writ-

ten into time slots of said second set of time slots in maintained mutual order.

In another embodiment, each incoming time slot to be switched by the node is tagged with a unique identifier, said identifier being translated directly into a physical slot number at the output port, for example using an identifier-to-slot mapper, said physical slot number being determined at channel set-up.

According to the invention, said read time slot data may be transferred within said node using allocated time slots of an internal bitstream, said bitstream being divided into cycles which in turn are divided into time slots, said internal bitstream preferably being shared by several input and output ports. Such an internal bitstream simplifies the internal handling of the time slot data in the node. For example, if data is to be multicasted from one input port to several output ports, there is no need to make copies of the data to be switched since it will be transferred to all parts of the node having connections with the other bitstreams. As is also understood, the term internal bitstream does not necessarily mean that the bitstream or the bitstream carrying medium must reside physically inside a switch circuit or the like, but may be arranged peripheral to the circuit, however still being used for the transfer of data between different ports of the switch.

As is understood, a bitstream at an input port of the switch node may be terminated at the switch node, as is the case if the switch node is a tail end node, or it may continue past the switch node to reach other nodes located downstream with respect to the switch node. Also, a bitstream at an output port of the switch node may origin from the switch node, as is the case if the switch node is a head end node, or it may origin from other nodes located upstream with respect to the switch node.

Of course, the invention is not restricted to, for example, DTM networks but can be used in any circuit

switched synchronous time division multiplexed network with cycles and slots of arbitrary sizes.

Furthermore, the present application forms one of a series of three applications referring to related inventive ideas, filed on the same day and having the same title, the descriptions of the other two thus hereby being incorporated by reference.

The above mentioned and other aspects and features of the invention will be more fully understood from the following description, with reference to the accompanying drawings, of exemplifying embodiments thereof.

Brief description of the drawings

Exemplifying embodiments of the invention will be described below with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows the structure of a bitstream of a circuit switched time division multiplexing network;

Fig. 2 schematically shows a switch node in a first embodiment of the invention;

Fig. 3 schematically shows a switch node in a second embodiment of the invention;

Fig. 4 schematically shows a switch node in a third embodiment of the invention; and

Fig. 5 shows an example of the internal structure of the selection means included in the switch node of the present invention.

Detailed description of preferred embodiments

With reference to Fig. 1, the structure of the time multiplexed bitstreams in a circuit switched synchronous time division multiplexing network, according to the present invention, is shown. The bandwidth of each wavelength, i.e. each bitstream, is divided into fixed rate, for example 125 μs, cycles or frames. Each frame is in turn divided into fixed size, for example 64 bits, time

slots. The number of time slots within a frame thus depends on the network's bit rate. Of course, the number of time slots 1-6 shown in the frame of the bitstream in Fig. 1 is merely illustrative, the actual number of slots within each frame being far greater.

The time slots are in general divided into two groups, control slots C and data slots D. The control slots C are used for control signaling between nodes of the network, i.e. for carrying messages between nodes for the internal operation of the network, such as for channel establishment, slot allocation, and the like. The data slots D are used for the transfer of user data between end users connected to said nodes.

In addition to said control slots and data slots, each cycle comprises one or more synchronization slots S used to synchronize the operation of each node in relation to each frame. Also, to make sure that the number of slots in one frame will not overlap a following frame, a guard band G is added after the last slot at the end of each frame. As indicated in Fig. 1, the bitstream cycle is repeated continuously.

Each node has access to at least one control slot C and to a dynamic number of data slots D on the bitstream used by said node. Each node uses its control slot C to communicate with other nodes within the network. The number of data slots D allocated to each node depends upon the transfer capacity requested by the end users served by the respective node. If the end users of a certain node require a large transfer capacity, the node will allocate more data slots for that purpose. On the other hand, if the end users of a certain node merely require a small transfer capacity, the node may limit its number of allocated data slots. Also, the number of control slots allocated to each node may be increased or decreased depending on the node's demand for signaling capacity. Hence, the allocation of both time slots and data slots to different nodes may by dynamically adjusted as the

network load changes. It is understood, that in this kind of circuit switching there is no header or address information embedded in the data stream.

Note, that in the basic embodiment, a switch according to the invention does not handle control time slots C any differently than data time slot D. As far as the switch is concerned, both control slot and data slots provide time slot data to be switched in accordance with switching instructions stored in the switch. However, a switch node controller, controlling the operation of the switch may be allocated to use one or more control and data slots for receiving and/or transmitting information regarding channel establishment, modification and termination, and to control the switching instructions of the switch based thereupon.

Fig. 2 shows a switch node 210 connected to three unidirectional optical fibers 214, 219 and 222 transferring a first bitstream 215, a second bitstream 220, and a third bitstream 223, respectively. As previously stated, and also indicated in Fig. 2, each of the bitstreams is divided into cycles and each of said cycles is divided into time slots.

The node is by means of a Switch Node Controller (SNC) 235 configured to switch data from time slots in the frame transferred by the first bitstream to time slots in one or both of the frames transferred by the second and the third bitstream. At set-up of a channel through the switch node, the SNC 235 is informed of which time slots in the first bitstream and which time slots in, for example, the second (and/or the third) bitstream, respectively, that are allocated to the channel, or circuit. The SNC 235 is connected to a slot data tagging table 240 and selection means 250, 251, all of which will be described below, the connections being illustrated in Fig. 2 with dotted lines. Slot data tagging means 242 are included in the switch node in order to tag the time slot data which is to be switched by the node.

The switch node includes first bitstream access means 225 for reading time slot data from time slots in said first bitstream. The first bitstream access means 225 includes a Medium Access Unit (MAU), a bit clock, a slot counter and a frame clock (neither of which is shown in the figure). The MAU enables the node to read the time slots being transferred by the first bitstream. The bit clock is synchronized to the bitrate of the bitstream 215 transferred by the fiber 214 and used as input to the slot counter. The slot counter counts the number of slots transferred by the fiber 214 and is cyclically restarted by the frame clock at the start of each new cycle.

The slot data tagging table stores identifiers, or tag numbers. The information in the slot data tagging table is either fixed, that is a certain entry always has a certain tag number, or, the SNC 235 stores information in the slot data tagging table 240 at channel, or circuit, set-up. In the latter case the tag number at an entry is dependent upon which channel a time slot in the first bitstream is allocated to. The tag number may in this case be chosen to comprise information relating to the identification of said channel. Each time slot in the first bitstream read by the MAU included in the first access means has a corresponding entry in said table, and each entry that represents a time slot carrying data to be switched by the switch node is associated with a tag number.

In Fig. 2, only seven entries corresponding to cycles with seven time slots have been indicated in the slot data tagging table 240, but, as described earlier with reference to Fig. 1, a cycle in a bitstream will in practice contain a far greater number of slots and, thus, the table a far greater number of corresponding entries. The empty entries of the table, corresponding to time slots number 4 and 6, indicates that the corresponding time slot data are not to be switched by this switch node.

The counter value of the slot counter included in the first access means is used to address entries in the slot data tagging table 240. The information associated with an entry, and thus with each cyclically occurring time slot position, is outputted from the table and transferred to the slot data tagging means 242. For each time slot read by the MAU that has information in the form of a tag number associated with it in the slot data tagging table 240, the time slot data is transferred from the time slot of the first bitstream to the slot tagging means 242. Said slot tagging means will tag the tag number, corresponding to the time slot and outputted from said slot data tagging table, onto the time slot data. The tagged slot data is transferred further down the node to be received in connection with those parts of the switch node that are connected to the node external bitstreams.

The selection means 250, for example having the configuration as will be described later with reference to Fig. 5, will, based upon the received tag number, select a position in a cycle, or frame, of the second bitstream 219. Said selected position, corresponding to one of the time slots allocated to the channel in the second bitstream, will be used for addressing a frame buffer 260. Upon addressing the frame buffer, the time slot data transferred from the slot data tagging means, either directly or via the selection means, will be stored at the address location selected by the selection means 250.

Correspondingly, the selection means 251, will, based upon the received tag number, select a position in a frame of the third bitstream 222. Said selected position, corresponding to one of the time slots allocated to the channel in the third bitstream, will be used for addressing a frame buffer 261. Upon addressing the frame buffer, the time slot data transferred from the slot data tagging means, either directly or via the selection

means, will be stored at the address location selected by the selection means 251.

Included in the switch node are also second and third bitstream access means, 230 and 231, for writing time slot data to time slots in said second and third bitstream, respectively. Since these two bitstream access means have the same structure and the same functionality, only one of them will be described. The second bitstream access means 230 includes a Medium Access Unit (MAU), a bit clock, a slot counter and a frame clock (neither of which is shown in the figure). The MAU enables the node to have access to the time slots being transferred by the second bitstream. The bit clock is synchronized to the bitrate of the bitstream 220 transferred by the fiber 219 and used as input to the slot counter. The slot counter counts the number of slots transferred by the fiber 214 and is cyclically restarted by the frame clock at the start of each new cycle. The counter value of the slot counter is used to address entries in the frame buffer 260. The time slot data stored in said frame buffer at a specific entry is transferred to the MAU, which MAU then writes the time slot data in a time slot having a position in a cycle of the second bitstream corresponding to the entry of the frame buffer.

For example, assume that time slot data in the, for each frame, recurring time slot number 5, allocated to a certain channel, in the first bitstream 215 is to be switched to a recurring time slot number 17, allocated to the channel, in the second bitstream 220 as well as to a recurring time slot number 23, allocated to the channel, in the third bitstream 223.

When the first bitstream access means 225 reads time slot number 5 from a cycle of the first bitstream 215, its slot counter value will address the fifth entry of the slot data tagging table 240. At this entry, a tag, in this case denoted T5, is either constantly stored or has been stored by means of the SNC 235 during channel set-

up. The tag T5 will be outputted and transferred to the slot data tagging means 242. Meanwhile, the time slot data read from time slot number 5 of the first bitstream is also transferred to said slot data tagging means. The slot tagging means 242 will then tag the tag number T5 onto the time slot data and transfer the tagged slot data further down the node to be received in connection with those parts of the switch node that are connected to the second and the third bitstreams.

The selection means 250 and 251 will, based upon the received tag number, and if configured to make a selection for that specific tag number, select a position number for a time slot allocated to a channel in the second and the third bitstream, respectively. The selection means will use the time slot position number to address the corresponding entry in the frame buffer 260 and 261m respectively, at which entry the time slot data, to which the tag number was tagged, is stored. In this case, the selection means 250 will select time slot number 17 as a result of the received tag number T5. The selection means 250 then addresses the seventeenth entry of the frame buffer 260, at which entry the data, to which T5 was tagged, is stored. Correspondingly, the selection means 251 will in this case select time slot number 23 as a result of the received tag number T5. The selection means 251 then addresses the twenty-third entry of the frame buffer 261, at which entry the data to which T5 was tagged is stored.

This procedure is repeated continuously for all time slots of the first bitstream, at the start of each new cycle in the first bitstream the slot counter is restarted by the frame clock.

At the same time, the second bitstream access means 230 will write time slot data to time slots in the second bitstream. When its slot counter has been restarted by its frame clock at the start of a new cycle in the second bitstream, the counter value will be one, and the slot

counter will address the first entry of the frame buffer 260. The data stored in the frame buffer at this first entry will be outputted and transferred to the MAU included in the second bitstream access means. The MAU will write the transferred data in the first time slot of the frame currently being transferred by the second bitstream. Thus, when the slot counter has been incremented to 17, the data transferred by the fifth time slot in the first bitstream will have been switched to the seventeenth time slot in the second bitstream. This procedure is repeated until the slot counter of the second bitstream access means is once again restarted by the frame clock. Correspondingly, in a similar manner as described with reference to the second bitstream access means 230, the third bitstream access means 231, having the same structure and functionality as the second bitstream access means 230, will utilize frame buffer 261 and write the data transferred by the fifth time slot in the first bitstream to the twenty-third time slot in the third bitstream.

Thus, this example has shown how multicast is achieved in a first embodiment of the present invention. Of course, if either one of the selection means 250 or 251 is configured with information that does not select a time slot position number on the basis of the tag number T5, multicast will not be realized.

In Fig. 3 a second embodiment of the invention is shown. The switch node 310 is again connected to three unidirectional optical fibers 314, 319 and 322 transferring a first bitstream 315, second bitstream 320, and a third bitstream 323, respectively. The switch node also includes first bitstream access means 325, second bitstream access means 330 and third bitstream access means 331, a switch node controller 335, a slot data tagging table 340, a slot data tagging means 342 and a selection means 350 and 351 having previously been described with

reference to Fig. 2, and will not be further described with reference to this embodiment.

The switch node here includes preselection means 345 for selecting which of said second and third bitstream that time slot data read from the first bitstream is to be transferred to. This preselection is done based upon the tag which the slot data tagging means 342 has tagged to the time slot data. The preselection means are configured by the SNC 335 at channel set-up. If the preselection means determines, based on the tag, that the tagged data should be transferred towards both the second and the third bitstream, a copy is made of the time slot data and this copy is provided with the same specific tag number as the original time slot data. One set of tagged time slot data is then transferred from the preselection means 345 towards the output port connected to the second bitstream and one set of tagged time slot data is transferred from the preselection means 345 towards the output port connected to the third bitstream. If the preselection means determines, based on the tag, that the tagged data only should be transferred towards one of the bitstreams, the tagged time slot data is only transferred towards the output port connected to that bitstream.

Thus, the selection means 350 will in this embodiment receive the tag number from the tagged time slot data transferred from the preselection means 345. Also, a received tag number will always result in a time slot position number being selected, since the preselection means already have determined that a time slot data should be transferred towards the output port connected to the second bitstream, and thus that a time slot in the second bitstream should be selected. Upon addressing the frame buffer 360, the time slot data onto which the tag was tagged will be, either directly from the preselection means or via the selection means 350, stored at the address location selected by the selection means 350. Correspondingly, the selection means 351 will also

receive the tag number from the tagged time slot data transferred from the preselection means 345. Upon addressing the frame buffer 361, the time slot data onto which the tag was tagged will be, either directly from the preselection means or via the selection means 350, stored at the address location selected by the selection means 351. If the preselection means have determined that the tagged data should be transferred towards both the second and the third bitstream, the selection means 350 and 351 will receive the same tag and the same time slot data will be stored in the corresponding buffers 360 and 361.

In correspondence to the previous description of the second and third bitstream access means with reference to Fig. 2, the second and third bitstream access means, 330 and 331, respectively, of Fig. 3 will address entries of its respective frame buffer, 360 and 361. The time slot data stored at a specific entry of the frame buffer 360 will be written into a time slot having a position in a cycle of the second bitstream corresponding to the entry of the frame buffer 360. Correspondingly, time slot data stored in the frame buffer 361 will be written into time slots of the third bitstream.

In Fig. 4 a third embodiment of the invention is shown. The switch node 410 is again connected to three unidirectional optical fibers 414, 419 and 422 transferring a first bitstream 415, second bitstream 420, and a third bitstream 423, respectively. The switch node also includes first bitstream access means 425, second bitstream access means 430, third bitstream access means 431, a switch node controller 435, a slot data tagging table 440, a slot data tagging means 442 and selection means 450 and 451 having previously been described with reference to Fig. 2 and will not be further described with reference to this embodiment.

The switch node here includes a medium on which an internal bitstream 470 propagates. The internal bitstream, which is divided into cycles which in turn are

divided into time slots, is used for transferring time slot data within the switch node. The internal bitstream propagates on said medium within the node in such way that it can be accessed in connection with both output ports, being connected to the node external bitstreams, of the switch node.

A first internal bitstream access means 445, having read access to the internal bitstream, is situated in connection with the part of the switch that is connected to the second bitstream. Correspondingly, a second internal bitstream access means 446, having read access to the internal bitstream, is situated in connection with the part of the switch connected to the third bitstream.

The slot tagging means 442 will transfer the tagged slot data, which slot data was read from a time slot in the first bitstream and which tag was received from the slot data tagging table 440 and tagged to the read time slot data, into one or two time slots of the internal bitstream. The tag is either concatenated with the slot data and stored in the same time slot of the internal bitstream, or the tag and the slot data are stored in two separate time slots being separated with a predefined number of slots, or the tag is transferred by one or more predefined allocated time slots in said internal bitstream while the slot data is transferred by another time slot of the internal bitstream.

In connection with the output port connected to the second bitstream, the first internal bitstream access means 445 will read a tag, and the time slot data onto which the tag is tagged, from time slots of the internal bitstream. The tag will be further transferred to the selection means 450 which will, based upon the received tag number, and if configured to make a selection for that specific tag number, select a position number for a time slot in the second bitstream. The selection means will use the position number to address the corresponding entry in the frame buffer 460. The time slot data onto

which said tag is tagged will be transferred from the first internal bitstream access means and stored in the frame buffer at said entry.

Correspondingly, in connection with the output port connected to the third bitstream, the second internal bitstream access means 446 will read a tag, and the time slot data onto which the tag is tagged, from time slots of the internal bitstream. The tag will be further transferred to the selection means 451 which will, based upon the received tag number, and if configured to make a selection for that specific tag number, select a position number for a time slot in the third bitstream. The selection means will use the position number to address the corresponding entry in the frame buffer 461. The time slot data onto which said tag is tagged will be transferred from the first internal bitstream access means and stored in the frame buffer at said entry.

In correspondence to the previous description of the second and third bitstream access means, with reference to Fig. 2, the second and third bitstream access means, 430 and 431, respectively, will address entries of its respective frame buffer, 460 and 461. The time slot data stored at a specific entry of the frame buffer 460 will be written into a time slot having a position in a cycle of the second bitstream corresponding to the entry of the frame buffer 460. Correspondingly, time slot data stored in the frame buffer 461 will be written into time slots of the third bitstream.

With reference to Fig. 5, an example of the structure of the selection means according to the present invention will now be described. The selection means 550 basically includes one table, a tag-to-slot table 540. The tag-to-slot table has entries that are addressed by the tag which earlier was tagged by the slot data tagging means to the time slot data read from the first bitstream. Each entry of the tag-to-slot table contains data referring to a time slot position number in the bitstream

connected to the output port to which the selection means belong. The information in the tag-to-slot table is either fixed, that is a certain entry always has a certain time slot position number, or, the SNC stores information in the tag-to-slot table at channel, or circuit, set-up. In the latter case the time position number stored in the table is dependent upon the information relating to an identification of a channel that a tag may comprise. The selection means 550 uses the time slot position number to address the frame buffer, as described hereinbefore.

The information stored in the tag-to-slot table of the selection means, together with the information stored in the preselection means if such is present in the switch node, may be chosen in such way that the switch node multicasts time slot data from the first bitstream to the second and the third bitstream. In this case two sets of selection means at different output ports have tag-to-slot tables configured to select time slot positions in the bitstreams connected to respective output ports as a response to the same tag number.

As is understood, the description above of exemplifying embodiments of the invention has been made in order to provide a better understanding thereof. Of course, an actual switch will incorporate elements not shown in the figures, and may also be realized using other components than the ones specifically described herein. For example, at different locations in the switch, further frame buffers, multiplexing means, and the like, may be provided to facilitate the desired operation.

As is understood by those skilled in the art, even though the invention has been described with reference to exemplifying embodiments thereof, different alterations and combinations may be made thereof within the scope of the invention, which is defined by the accompanying claims.

CLAIMS

1. A method for switching data, in a switch node, between bitstreams of a circuit switched synchronous time division multiplexing network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots, comprising the steps of:

tagging time slot data read from a time slot of a first bitstream of said bitstreams with an identifier; and

selecting, for each one of at least a second and a third bitstream of said bitstreams, whether or not said time slot data is to be transmitted thereto and, if so, into which time slot thereof, based upon said identifier.

2. A method as claimed in claim 1, wherein said selecting step comprises:

first selecting which of said at least a second and a third bitstream that said time slot data is to be transferred to based upon said an identifier;

then selecting, for each one of the first selected bitstreams, a respective time slot for said time slot data to be written into based upon said identifier.

3. A method as claimed in claim 1 or 2, comprising tagging each read time slot data with a respective specific tag number, and tagging optionally provided copies of said read time slot data with the same specific tag number, said tag number forming said identifier.

4. A method as claimed in claim 1, 2, or 3, wherein said time slot data and said identifier are transferred within said node using time slots of an internal bit-stream.

5. A method as claimed in claim 4, wherein said time slot data is concatenated with said identifier.

6. A method as claimed in claim 4, wherein said time slot data is transferred in a time slot, in said internal bitstream, which has a predetermined position in relation to the time slot in which said identifier is transferred.

7. A method as claimed in claim 4, wherein said identifier is transferred by one or more predefined allocated time slots in said internal bitstream.

8. A method as claimed in any one of the preceding claims, wherein an isochronous channel is established on said bitstreams, said channel comprising a first set of time slots in the first bitstream and a second set of time slots in the second bitstream, said method comprising the steps of:

reading time slot data from a time slot of said first bitstream;

identifying the channel associated with said time slot;

incorporating information as to the identification of said channel into said identifier;

selecting a time slot of said second bitstream based upon the channel information provided by said identifier, said selected time slot thus being a time slot of said second set of time slots; and

writing said time slot data into said selected time slot in said second bitstream.

9. A method as claimed in claim 8, wherein said selecting step comprises selecting the next available time slot of said channel on said second bitstream.

10. A method as claimed in claim 8 or 9, wherein time slot data from each time slot of said first set of time slots are tagged with the same tag number, said tag number forming said identifier.

11. An apparatus for switching data between bitstreams of a circuit switched synchronous time division multiplexing network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots, comprising:

associating means (240, 242; 340, 342; 440, 442) for tagging time slot data read from a time slot of a first bitstream of said bitstreams with an identifier; and

selecting means (250, 251; 345, 350, 351; 450, 451) for selecting, for each one of at least a second and a third bitstream of said bitstreams, whether or not said time slot data is to be transmitted thereto and, if so, into which time slot thereof, based upon said identifier.

12. An apparatus as claimed in claim 11, wherein said associating means are provided at an input port of said switch, said input port providing at least read access to said first bitstream.

13. An apparatus as claimed in claim 11 or 12, wherein said selecting means are provided at the respective output port of said switch, each of said output ports providing at least write access to the respective bitstream of said at least a second and a third bitstream.

14. An apparatus as claimed in claim 11, 12, or 13, wherein said associating means are arranged to tag each time slot data with a respective specific tag number, and wherein optionally provided copies of said read time slot data are provided with the same specific tag number, said tag number forming said identifier.

15. An apparatus as claimed in claim 11, 12, 13 or 14, wherein said selecting means comprises:

first selecting means (345) for selecting which of said at least a second and a third bitstream that said time slot data is to be transferred to based upon said identifier;

second selecting means (350, 351) for then selecting, for each one of the first selected bitstreams, a respective time slot for said time slot data to be written into based upon said identifier.

16. An apparatus as claimed in any one of claims 11-15, wherein said time slot data and said identifier are transferred within said apparatus using time slots of an internal bitstream (470).

17. An apparatus as claimed in claim 16, wherein said time slot data is concatenated with said identifier.

18. An apparatus as claimed in claim 16, wherein said time slot data is transferred in a time slot, in said internal bitstream, which has a predetermined position in relation to the time slot in which said identifier is transferred.

19. An apparatus as claimed in claim 16, wherein said identifier is transferred by one or more predefined allocated time slots in said internal bitstream.

20. An apparatus as claimed in any one of claims 11-19, wherein an isochronous channel is established on said bitstreams, said channel comprising a first set of time slots in the first bitstream and a second set of time slots in the second bitstream, said method comprising the steps of:

bitstream access means for reading time slot data from a time slot of said first bitstream;

means for identifying the channel associated with said time slot;

means for associating information as to the identification of said channel into said identifier;

means for selecting a time slot of said second bitstream based upon the channel information provided by said identifier, said selected time slot thus being a time slot of said second set of time slots; and

bitstream access means for writing said time slot data into said selected time slot in said second bitstream.

21. An apparatus as claimed in claim 20, wherein said associating means is provided to tag each time slot data from each time slot of said first set of time slots with the same tag number, said tag number forming said identifier.

22. An apparatus as claimed in claim 20 or 21, wherein said selecting means are provided to select the next available time slot of said channel on said second bitstream.

23. An apparatus as claimed in claim 20, 21, or 22, wherein said selecting means are provided to select time slots of said second set of time slots so that the writing of said time slot data from time slots of said first set of time slots maintains the mutual time slot data order within said channel.

ABSTRACT

The present invention refers to a method and an apparatus for switching data between bitstreams of a circuit switched synchronous time division multiplexing network, each of said bitstreams being divided into cycles and each of said cycles being divided into time slots. According to the invention, time slot data read from a time slot of a first bitstream of said bitstreams is tagged with an identifier. Then, for each one of at least a second and a third bitstream of said bitstreams, said identifier is used for selecting whether or not said time slot data is to be transmitted thereto and, if so, into which time slot thereof.

(Elected for publication: Fig. 2)

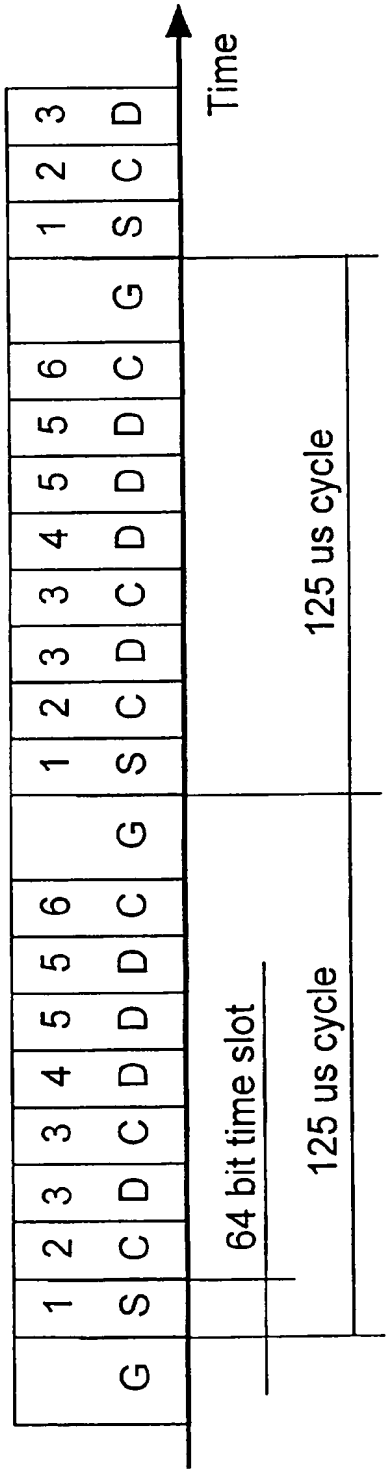

Time
G
1
S
2
C
3
D
3
C
4
D
5
D
5
D
6
C
G
1
S
2
C
3
D
3
C
4
D
5
D
5
D
6
C
G
1
S
2
C
3
D
64 bit time slot
125 us cycle
125 us cycle

FIG. 1

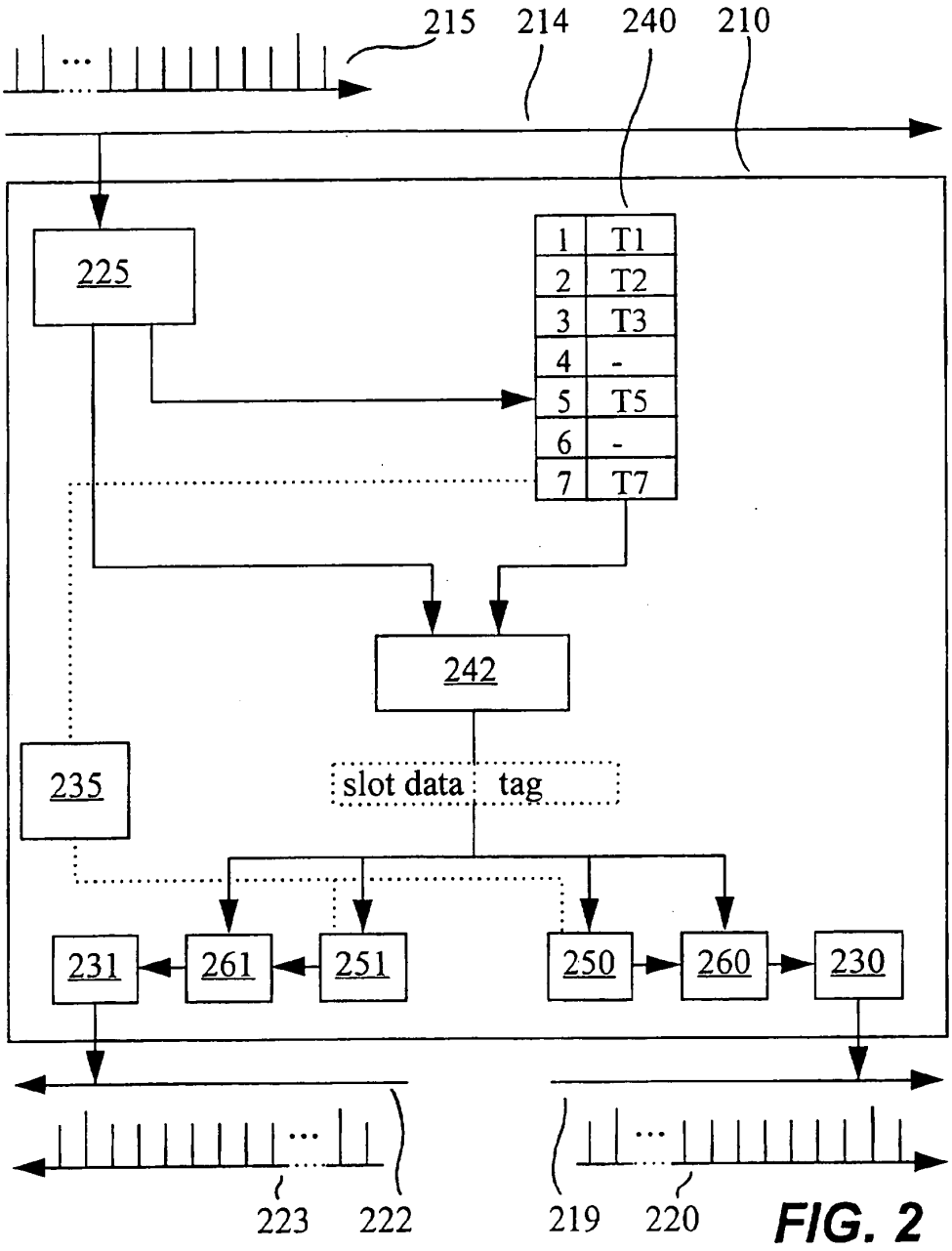

215
214
240
210
225
1 T1
2 T2
3 T3
4 -
5 T5
6 -
7 T7
242
235
slot data
tag
231
261
251
250
260
230
223
222
219
220

FIG. 2

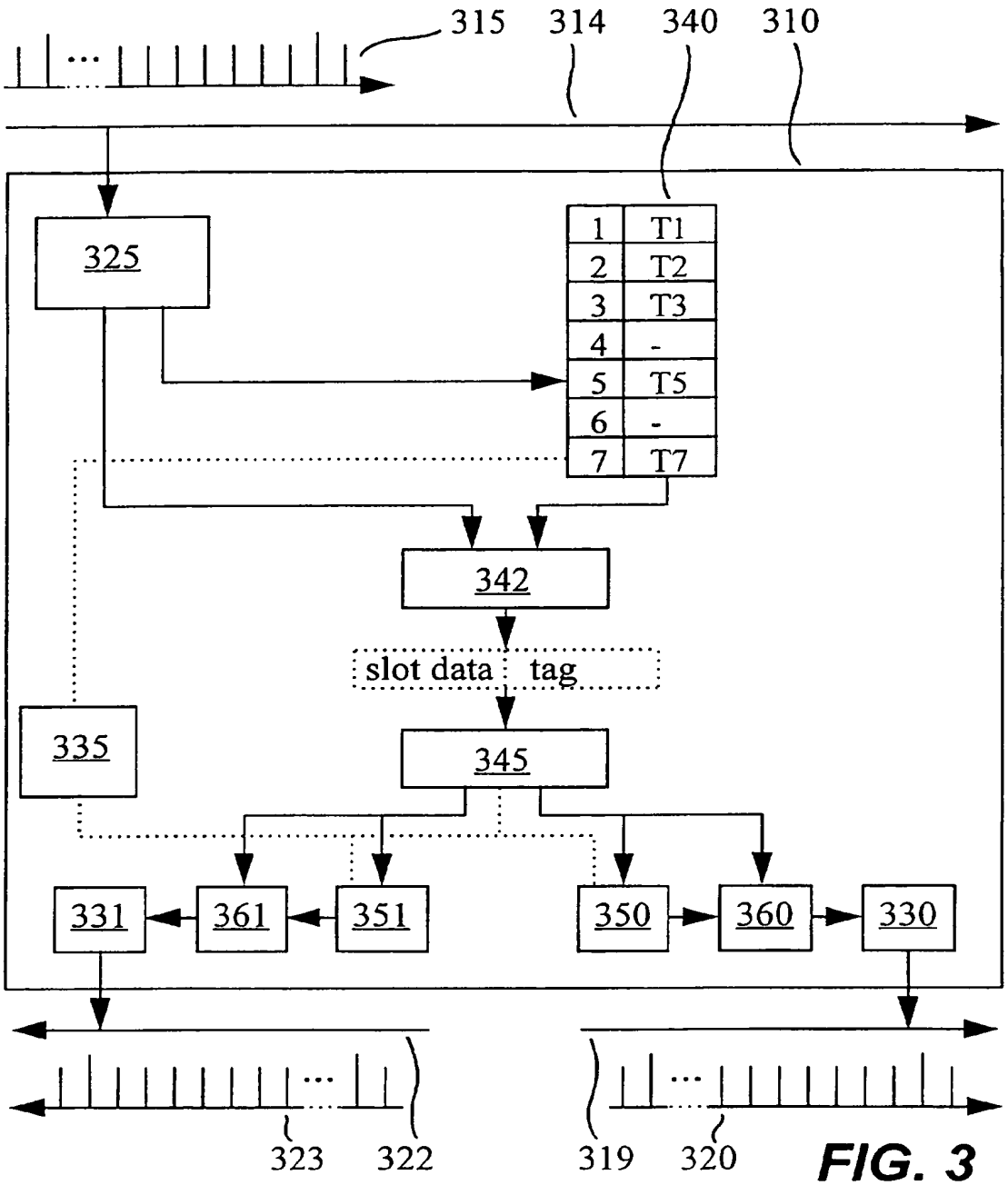
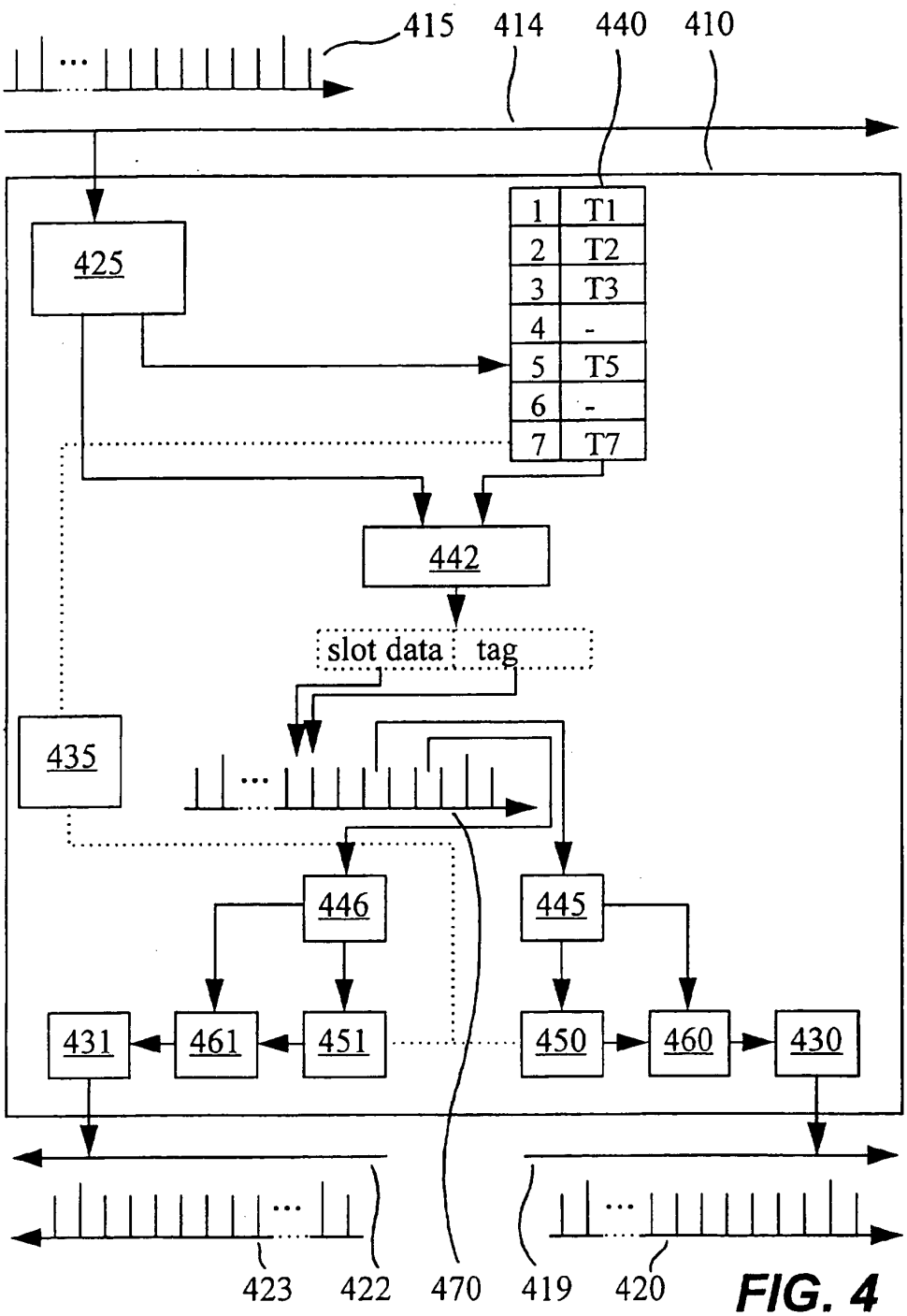

315
314
340
310
325
1 T1
2 T2
3 T3
4 -
5 T5
6 -
7 T7
342
slot data
tag
335
345
331
361
351
350
360
330
323
322
319
320

FIG. 3


415
414
440
410
425
1 T1
2 T2
3 T3
4 -
5 T5
6 -
7 T7
442
slot data
tag
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446
445
431
461
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423
422
470
419
420

FIG. 4

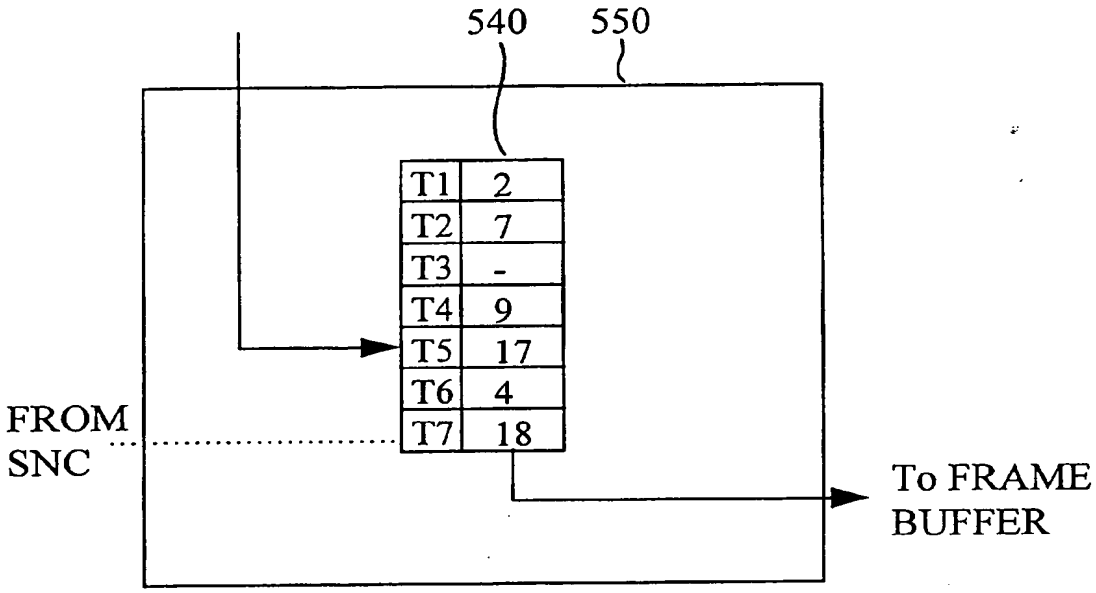

FIG. 5